

thin film transistor,

said thin film transistor comprising:

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a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

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2. (Amended) The device of claim 1 wherein said thin film transistor is an inverted-staggered thin-film transistor.

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3. (Amended) The device of claim 1 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

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5. (Twice Amended) A semiconductor device comprising:
a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;
a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and
a thin-film transistor provided on said planarized surface of said resinous layer;
an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and
at least one pixel electrode provided on said interlayer insulating layer,
said thin film transistor comprising:

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a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

6. (Amended) The device of claim 5 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

10. 11. (Three Times Amended) A semiconductor device comprising:
a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

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a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

said thin film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises microcrystalline silicon.

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(Three Times Amended) A semiconductor device comprising:

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a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

said thin film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

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11. 13. (Amended) The device of claim 11 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

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13.
(Amended) The device of claim 12 wherein said first resinous substrate

16. 18. comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

16. 18. (Three Times Amended) A semiconductor device comprising:
a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a ferroelectric liquid crystal layer therebetween;
a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and
a thin film transistor provided on said planarized surface of said resinous layer;
and
an interlayer insulating layer comprising resinous material provided over said thin film transistor,
said thin film transistor comprising:
a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and
a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,
wherein said channel formation region comprises amorphous silicon.

18. 20. (Amended) The device of claim 18 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

19. 21. (Amended) The device of claim 18 wherein said resinous layer comprises a

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material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

E9 21. ~~23~~. (Three Times Amended) A semiconductor device comprising:
a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween;
a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and
a thin film transistor provided on said planarized surface of said resinous layer;
an interlayer insulating layer comprising a resinous material provided over said thin-film transistor;
at least one pixel electrode provided on said interlayer insulating layer,
said thin film transistor comprising:
a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and
a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,
wherein said semiconductor layer comprises amorphous silicon.

E10 23. ~~21~~. (Amended) The device of claim ~~23~~ ²¹ wherein said resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

E11 27. ~~28~~. (Three Times Amended) A semiconductor device comprising:
a first resinous substrate having an uneven surface, a second resinous substrate

opposed to said first substrate, and a ferroelectric liquid crystal layer therebetween;

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a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said channel formation region comprises microcrystalline silicon.

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29.3b. (Amended) The device of claim ²⁷~~28~~ wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

30.31. (Amended) The device of claim ²⁷~~28~~ wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

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31.3b. (Three Times Amended) A semiconductor device comprising:
a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween;
a resinous layer provided on said uneven surface of said resinous substrate and

having a planarized surface; and

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a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,
said thin-film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises microcrystalline silicon.

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33. ~~35~~³¹. (Amended) The device of claim ~~35~~³¹ wherein said resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

34. ~~36~~³¹. (Amended) The device of claim ~~36~~³¹ wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

Please add new claims 38-46 as follows.

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36. --38. (New) A semiconductor device comprising:
a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween, wherein

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said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween.

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39. (New) The device of claim 38 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

38. 40. (New) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first substrate, and a ferroelectric liquid crystal layer therebetween, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate

and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

said thin-film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween.

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41. (New) The device of claim 40 wherein said thin film transistor is an inverted-staggered thin-film transistor.

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42. (New) The device of claim 40 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

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43. (New) A semiconductor device comprising:
a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween, wherein said resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,
wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween.

42. 44. (New) The device of claim 43 wherein said thin film transistor is an inverted-staggered thin-film transistor.

43. 45. (New) The device of claim 44 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

44. 46. (New) The device of claim 45 wherein said pixel electrode comprises an indium tin oxide.--

REMARKS

Applicant would like to thank Examiner Guerrero for the very thorough consideration given the subject application. The Office Action of **June 18, 2001**, has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed. Claims 1-8 and 11-37 were pending in the present application prior to the aforementioned amendment. By the above Amendment, claims 1-3, 5, 6, 1-